Title: DIGITAL POWER CONTROLLER

5   FIELD OF THE INVENTION

This invention relates to power controllers and
more specifically relates to a power controller, using
digital implementation with such stand-alone features as
10   automatic shut down; dead time control, close to inductive
side driving; and filament connections.

BACKGROUND OF THE INVENTION

15   Power controllers are well known and normally
employ analog techniques. Digital techniques are normally
avoided where smooth control is desired, for example, in
controlling the dimming gas discharge lamps such as
fluorescent lamps in an electronic ballast.
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The present invention provides a novel digital
implementation for power control circuits, particularly
for the control of fluorescent lamp dimming.

25   Some limitations on analog power control systems
are:

I.   Inflexible driving algorithm

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Optimal driving of power switches (MOSFETs, bipolar, transistors, thyristers, IGBTs and the like) requires complex algorithms based on non-linear multiple stage and variable functions, with a variety of

5   predetermined parameters being chosen as the circuitry's physical parameters change.

For example, in the case of a fluorescent ballast power controller, flexible algorithms are desired

10   to supply special loads when:

a)   a complex working regime for fluorescent lamps including the preheat startup operation is needed.

b)   Non-linear or special operation requirements for the fluorescent lamp complying to its V/I

15   working curve, and as a function of the dimming decision table to provide the best operation at all light levels.

c)   Flexibility to enable use of different lamp configurations (types and numbers of lamps) and different main voltages.

20

II.   The number of electronic circuits increases as number of control function increases. If silicon implementation is feasible, it requires a large silicon overhead.

25

III.   No decision tables

An analog solution does not provide "IF-THEN" decisions. It only provides "YES - NO" decisions using analog comparators and only linear predetermined

30   algorithms. For example: voltage controlled oscillator (VCO) for frequency modulation

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(FM) or pulse width modulation (PWM) zero to max., pulse control, etc.

IV.   No parameters set tables

5   This has to do with different lamp configurations, in the case of a fluorescent lamp ballast, but also with many other decisions made by the controller in every state of its operation. One specific example is the time response of the lamp current loop being different

10   at high level or low level as well as during transient or at steady state operation.

BRIEF DESCRIPTION OF THE PRESENT INVENTION

15   The present invention provides a number of novel improvements which can be integrated into a simple system, or, in some cases can be used singly in a stand- alone circuit. These improvements are:

20   I.   Programmable predetermined fixed internal parameters can be programmed by the designer, by means of simple MMI, adapting control loops to the desired operation regimen and power circuit, while protecting the power circuit from damage if running it under "non-legal"

25   settings. This technique allows on-the-spot matching of control to power circuit, instead the tedious and costly procedure common in digital signal processing (DSP) devices that requires programming of dedicated software and back and forth adapting of control to power.

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The predetermined fixed internal parameters above refer to a set of numbers and tables intended for:

- limits, constants, parameters and signed coefficients included in the control loop algorithm; and

5

- addressing/identification; etc.

Examples of the above are:

1. to normalize to "real" signals;

10

2. to create the limits for the "IF - THEN" algorithm.

3. to adapt to the designed configuration and the work regimen of the ballast.

15

II. Programmable predetermined parameter internal power configuration tables are provided.

III. An externally programmable new parameters table is provided that can be set for a specific

20 application that cannot use the already existing tables (for example: an EEPROM function).

IV. Software substitutes may be used for analog circuits.

25

V. An application specific integrated circuit (ASIC) handles, in principle, an indefinite quantity of functions with an insignificant amount of silicon. Thus, all possible components/circuits/algorithms are integrated

30 on the same silicon. This provides a simple low cost and enhanced solution with all the flexibility provided by

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software. The integration provides high noise immunization, eliminates intercircuit interfacing components, shares circuitry elements and allows dramatic space reduction.

5

VI. A gate array is provided which includes the fast algorithms or the fast portion of them, like:
1. Center Tap;
2. Zero, minimum and maximum current of the power factor corrector (PFC);
10
3. Generation of driver pulses.

VII. A microcomputer and the gate array share functions that are being carried out in parallel.

15

VIII. A very low-end microprocessor processes all the jobs by time-sharing instead of using the super-scalar processor used in DSPs.

IX. A gate array carries out all of its
20 assignments in parallel. Functionally, the assignments operate in parallel and require separate gate array sections or blocks for each one.

X. The microprocessor manages the gate array
25 operation, among others.

XI. The gate array receives input from monitoring nets and operates the immediate algorithm protections. In the case of fluorescent lamp dimming, the
30 job is done by using all the main ASIC elements A/D, microprocessor, and gate array. In the

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embodiment described, the gate array also carries out watchdog functions.

XII. The microprocessor monitors protections being operated and takes care of long term actions.

XIII. In general, the functions constructed by fast and slow sub-functions are handled as follows:

The algorithm implemented in the gate array carries out the fast sub-functions which include fast pulses or actions. The sub-functions which require processing or actions that can be carried out during a slower mode, are carried out by the microprocessor. The novel structure and process of the invention provide a programmable integrated digital control module which can be used for a dimming fluorescent ballast. The control module features are:

a) Combines the Integrated Digital Control Dimmable Electronic Ballast (DEB) ASIC on a programmable printed circuit board product for new lighting ballast designs and evaluation suitable for low to medium volume production.

b) A large number of "on board" programmable, for example, 14, parameters define preheat, absolute light-level and dimming range.

c) An EEPROM enables the control parameters described above to use a single hardware platform for multiple lamps, diverse operation regimens and applications.

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d)   Integrated software defaults predefined
parameters to a 2-lamp 32w/36w lamp drive for 120/230V a-c
line/mains.

5   e)   Incorporates all dimming ballast controls,
including power conversion, into a single digital ASIC
with multi-mode closed-loop control and pulse-by-pulse
bridge protection.

10   f)   A modified critical-mode boost PFC control
achieves lowest total harmonic distortion (THD) at all
light levels.

g)   A series resonant lamp inverter control
15   achieves less than 1% current-level control as required
for architectural dimming fluorescent ballasts.

h)   Module flexibility speeds product redesign
and field testing in advance of custom ASIC software
20   specification suitable for high-volume ballast products.

A large number of other features can be
incorporated into the novel system of the invention, as
integral parts of the system, or as stand alone features
25   which could be incorporated into any ballast control
circuit. These include:
1.   A novel shut down circuit for turning off
power to ballast in response to the sensing of a common
mode high frequency current which exceeds a given value.
30   In particular, an added winding is wound on the common
mode choke to sense a high frequency

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ground fault current and turn off power to the ballast in
response thereto.

       2.   A novel circuit for connecting two or more
filaments of two or more gas discharge lamps, particularly

5   fluorescent lamps, in parallel so that removal of any lamp
breaks that circuit while permitting the voltage applied
to the lamp to be reduced for dimming. In particular, a
series/parallel circuit is provided which enables
energization of the lamp filaments with a half wave

10   rectified DC.

       3.   A control arrangement for DC to AC
inverters for driving non-linear loads such as electronic
ballasts for high pressure and low pressure gas discharge
lamps, resonant power supplies and laser power supplies

15   and the like, wherein the control scheme employs both
variable pulse width and frequency modulation, driving the
load as close to resonance as possible but on the
inductive side of resonance. Both the high side and low
side switches of the bridge (half or full wave) are

20   independently controlled in this arrangement.

       4.   A novel protection circuit for a bridge
connected (half or full wave) inverter which supplies a
resonant load such as a resonant electronic ballast for
gas discharge lamps, which forces a dead-time during which

25   no switch is driven in conduction without limiting the
performance of the circuit. The point at which a dynamic
dead-time begins is sensed by sensing the point where
current collapses to zero in a capacitive timed circuit
case. The sensing circuits may sense inductor current

30   using a current transformer or shunt resistor, by sensing
the current through

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the switching devices, by sensing the bridge voltage or by sensing the bridge voltage dv/dt.

According to the present invention, an electronic ballast for a gas discharge lamp is provided in which the electronic ballast has an input a-c circuit, a common mode inductor for connecting said input a-c circuit to a bridge connected rectifier, an inverter circuit including a high side switch and a low side switch which is coupled to the bridge connected rectifier, and a resonant circuit coupling the inverter circuit to and driving the gas discharge lamp. A monitor circuit is coupled to the common mode inductor for sensing a high frequency fault ground current, which has a frequency greater than the frequency of the input a-c circuit, to a ground connection. A controller circuit is coupled to the monitor circuit for turning off the inverter circuit or the power to the inverter circuit when the high frequency ground current exceeds a given value.

As another aspect of the present invention, an electronic ballast for at least two parallel connected gas discharge lamps removably mounted in a fixture is provided in which there is an inverter circuit, a resonant coupling circuit and at least two gas discharge lamps. The gas discharge lamps have first and second filaments. The resonant coupling circuit includes an inductor and a capacitor connected in series with the first and second filaments. First and second windings are coupled to the inductor and first and second diodes are connected in series with the first and second windings respectively and the first and second diodes respectively, whereby the disconnection of the lamps and the filaments from

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their fixtures opens the output circuit from the inverter
circuit.

As another aspect of the present invention, an
electronic ballast for a gas discharge lamp is provided in
5   which there is an input a-c circuit. An a-c filter is
connected to the input a-c circuit. A rectifier bridge is
connected to the a-c circuit for producing an output d-c
voltage from the a-c circuit input. An inverter circuit
including a high side switch and a low side switch is
10   connected in series at a node and connected across the
output of the inverter circuit and a load circuit is
connected to the node and includes the gas discharge lamp.
The high side and low side switches each comprise MOSgated
devices, and the like, having input control terminals
15   energizable to turn them on and off and each has a
parallel diode. A master control circuit applies suitably
timed control signals for alternately turning the high
side and low side switches on and off. A dynamic dead
time control circuit in provided in the master control
20   circuit for insuring only a short interval between the end
of current conduction by either the high side and low side
MOSgated devices, and the like, and the beginning of
conduction by the other by the control of the application
of controls signals to their control terminals. The
25   dynamic dead time control circuit is coupled to and
monitoring at least one of the current in the resonant
load, the current in the first and second switches, the
output voltage of the rectifier bridge or the rate of
change dv/dt of the bridge voltages, and adjusts the
30   application of turn on signals to the high side and

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low side switches for both capacitive and inductive
operations.

As still another aspect of the present
invention, an electronic control module for controlling
5   the operation of an electronic ballast for at least one
lamp is provided in which the control module has an
integrated circuit operable in accordance with control
information to drive a first switch and a second switch to
power the at least one lamp using a combination of pulse
10   width modulation and frequency modulation. A first memory
is coupled to the integrated circuit, the first memory
storing a plurality of parameters tables, each parameters
table having the control information for the integrated
circuit.

15   As yet another aspect of the present invention,
an integrated circuit for controlling the operation of an
electronic lamp ballast is provided in which a central
logic supervisor controls the overall operation of the
electronic lamp ballast. A dc/ac generator module is
20   coupled to the central logic supervisor and provides drive
signals for an inverter circuit, the inverter circuit
having a first switch and a second switch. A power line
communication module is coupled to the central logic
supervisor and receives dimming control data across a
25   power line. A power factor correction module is coupled
to the central logic supervisor and controls power factor
detection and correction for the electronic lamp ballast.

As another aspect of the present invention, a
method for controlling the dimming operation of an
30   electronic ballast is provided in which a current

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through a load coupled to the electronic ballast is
monitored and the current to maintain a dimming level is
controlled.

5   BRIEF DESCRIPTION OF THE DRAWINGS
              Figure 1 is a prior art electronic ballast
circuit which presents a hazard in the presence of a high
frequency, high voltage ground fault.

10   Figure 2 shows a novel circuit to provide high
frequency hazard protection and is an improvement of the
circuit of Figure 1.

              Figure 3 is a circuit diagram of a lamp ballast
15   with a known serial connection of lamp filaments.

              Figure 4 shows a circuit diagram of a lamp
ballast with a known parallel connection of lamp
filaments.
20

              Figure 5 shows an improvement of the circuit of
Figures 1 and 4 and is a novel circuit arrangement for a
lamp ballast employing a novel series/parallel connection
of filaments.
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              Figure 6 shows a known generic half-bridge
ballast circuit operated in a near resonance operation.

              Figure 7 shows the voltages and currents in the
30   circuit of Figure 6 on a common time base for a reactive
phase condition.

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Figure 8 shows the voltages and currents in the circuit of Figure 6 for a capacitive phase condition.

Figure 9 shows the circuit of Figure 6 adapted with a novel current sense protection circuit.

Figure 10 shows the circuit of Figure 6 with a novel voltage sense protection circuit.

Figure 11 shows the circuit of Figure 6 with a novel dv/dt sense protection circuit.

Figure 12 shows the curves of Figure 8, using a novel continuous reactive load mode of operation.

Figure 13 shows the curves of Figure 12, modified by a novel use of predicted minimum dead time.

Figure 14 shows a novel voltage sense protection circuit (Figure 10) for an electronic ballast.

Figure 15 is a block diagram of a preferred ASIC which can be used to control the circuit of Figure 14.

Figure 16 is a block diagram of a full control module using the circuits of Figures 14 and 15.

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Figures 17 and 17A show the curves for the
novel independent control of the high side and low
side switches of a DC/AC bridge inverter.

Figure 18 is a block diagram of the silicon
5   topology of the ASIC of Figures 14 and 15.

Figure 19 shows relevant voltage and current
curves produced by the ASIC of Figure 18.

Figure 20 is a diagram of light level versus
current in which the curve is divided into matched
10   segments of the conventional non-linear curve.

Figure 21 is an interconnect diagram of a
PLC Remote Controlled Dimmable Ballast.

Figure 21A is a schematic diagram of the
ASIC used in Figure 20.

15   Figure 22 shows the ASIC pin assignment for
Figures 20 and 21.

Figure 23 is a Wall Control Unit schematic
diagram for the diagram of Figure 21.

20   Figure 24 is a further electrical diagram of
the ballast control module of the invention.

Figure 25 is an electrical diagram of the
ballast platform with control module.

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DETAILED DESCRIPTION OF THE DRAWINGS

There is next described the various novel
features which can be combined with one another and/or can
stand alone. These are described in Sections I through V
5   hereinafter.

I.   The High Frequency Hazard Protection
      Circuit

10   Referring to the drawings in which like
reference numerals refer to like elements, Figure 1
schematically shows a prior art electronic ballast circuit
in which an AC input line is connected to a full wave
bridge connected rectifier circuit 30 through a common
15   mode choke 31. The windings of the common mode choke or
inductor 31 both have stray capacitances associated
therewith as shown. The output of bridge 30 may be
connected to a DC-to-DC power factor converter circuit 33
which has one output connected to the V_{ss} bus and another
20   output to the V_{cc} bus.

A high side switching MOSFET (or other MOS
controlled device such as an IGBT) Q_1 is connected to the
V_{cc} bus and a low side switching MOSFET Q_2 is connected to
25   the V_{ss} bus. MOSFETs Q_1 and Q_2 are suitably controlled to
alternately turn MOSFETs Q_1 and Q_2 on and off with
controlled frequency, duty cycle and/or phase delay.

Output node 35 is then connected to a resonant
30   load, which, in Figure 1, consists of

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blocking capacitor 40, inductor 41, parallel capacitor 42
and fluorescent lamp 45 having filaments 43 and 44.

5   The line conductors in Figure 1 are connected to
ground 46 through capacitors 47 and 48. A hazard exists
if, because of a ground fault or the like an individual 50
is connected between the circuit and ground.

The hazard caused by the low frequency (50/60
10   Hz) is generally treated with a residual current sensor
(not shown). However, the high frequency (20-100Khz)
voltage used in electronic ballasts might be dangerous
because the voltages are high (especially during the
ignition period) and the gas in the tube behaves like a
15   large capacitor.

Figure 2 shows the novel circuit for avoiding
the above hazard problem. In Figure 2, those parts which
are similar to those of Figure 1 have identical
20   identifying numerals. A novel additional winding 60 is
added to the common mode choke 31. Winding 60 is
connected through diode 61 to a controller 62 which is
adapted to sense a fault condition. If winding 60 senses
a common mode high frequency current higher than a safe
25   value, controller 62 applies a "shut-down" signal to
converter 33, thereby shutting down the DC/AC power
bridge. Details of a typical converter and DC/AC power
bridge which could be used with this invention are later
described herein.

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II. DC Filament Supply Circuit for Safe
     Parallel Lamp Operation.

         A fluorescent lamp has two filaments at its two
5   sides. Thus, in Figure 3, lamp 45 has filaments 43 and
     44. These filaments must be heated before the lamp 45 can
     be ignited, and must remain heated if one wishes to
     operate lamp 45 at a "Low Light" or dimmed condition.
     There are two principal connections for lamp filaments
10   used in electronic ballasts, a serial connection and a
     parallel connection. Figure 3 shows the serial
     connection.

         In this configuration the heating current flows
15   through the resonance circuit formed by inductor 41 and
     capacitor 42. Prior to ignition and during a phase the
     voltage on the lamp should be low (under the ignition
     voltage). Therefore the operating frequency should be
     significantly above resonance. At that frequency the
20   current is determined by inductor 41 and might be too low
     to produce adequate filament heating. At and after
     ignition the current through the filament is adequate.

         Figure 4 shows a prior art parallel connection
25   of filaments 43 and 44. In this configuration the
     inductor 41 has additional windings 70 and 71 which are
     used a supply a heating voltage to filaments 43 and 44
     (rather than a series) current. This circuit provides an
     adequate current through the full lamp operating mode, but
30   it has a serious drawback. That is, when a lamp is taken
     out of its housing, current still flows through the
     resonance

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circuit 41 and 42 and might damage the ballast especially
when it is used to drive two parallel lamps.

5   In accordance with the invention, and as shown
in Figure 5, a novel series/parallel connection is
provided. Thus, windings 70 and 71 of Figure 4 are
reconnected as shown and are connected to filaments 44 and
43 respectively through diodes 75 and 76 respectively.

10   This approach applies parallel heating to the
filaments and connects the lamp in such a manner that
pulling it out of the housing will open the lamp circuit.

           The result is a serial-parallel combination, the
15   parallel segment feeding the lamp 45 with a half wave
rectified DC wave form. The diodes 75 and 76 are
connected in such a manner that whenever the lamp 45 is
pulled out, current flow is blocked.

20   The connection of a second lamp 45 is shown in
phantom lines in Figure 5. Under this arrangement, the
removal of one of the lamps still allows the remaining
lamp (or lamps where more than two lamps are driven) to
operate. The removal of all lamps blocks the current
25   flow.

III. Protective Circuits for the Bridge
     Inverter.

        Figure 6 shows a "generic" half-bridge circuit
5   for driving any desired resonant load, such as an
    electronic ballast. The half-bridge consists of the high
    side and low side MOSgated devices, and the like, such as
    MOSFETs Q_1 and Q_2 respectively. MOSFETs Q_1 and Q_2 are shown
    with conventional parallel body diodes 80 and 81
10 respectively and load 82 can be any desired resonant load
    such as gas discharge lamp. Basically, the circuit of
    Figure 6 is a resonant topology and the work regime is
    near resonance; that is, close to the resonant frequency
    of inductor 41 and capacitor 42. The invention to be
15 described is suitable for any application in which a
    reactive current might flow through the bridge Q_1, Q_2.
    Note that everything described below applies to a full
    bridge topology as well as the half-bridge shown in Figure
    6.
20

        Figure 7 shows relevant voltages and currents in
    the circuit of Figure 6 on a common time axis when the
    excitation frequency of MOSFETs Q_1 and Q_2 is above the
    resonant frequency of inductor 41 capacitor 42 and load
25 82. In this condition the load is reactive. In Figure 7,
    line 100 is the HO signal to Q_1 and line 101 is the LO
    signal to Q_2. The bridge voltage at node 35 is shown by
    line 102 and the bridge current is shown by line 103.

30   At the end of each excitation cycle in Figure 7,
    the current 103 through the inductor 41 lags

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behind the excitation voltage 102. When the upper switch Q_1 is closed, a current flows into the inductor 41. When the upper switch Q_1 opens or turns off, the current must continue flowing through the inductor 41 and does so by flowing through the lower switch integral diode 81 as shown by line 104 in Figure 7. When the lower switch Q_2 closes Q_2, the integral diode 81 recovers from conduction at a zero voltage by a recombination of carriers effect only.

The same behavior described above applies to the half cycle controlled by lower switch conduction line 105.

The following can be observed:

1.   When upper switch Q_1 is turned off, the inductive current is steered to the lower switch integral diode 81 and the voltage 102 at the bridge swings immediately from Vdd to Vss.

2.   The current steered into the lower switch integral diode 81 collapses to zero while the lower switch Q_2 is closed.

3.   Simultaneous conduction of both upper and lower branches Q_1 and Q_2 and of the bridge is not possible.

The diagram of Figure 8 shows the behavior of the inverter bridge of Figure 6 when the excitation frequency is below resonance (and the load is

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therefore called capacitive). The various traces of
Figure 8 have the same numerals as those of Figure 7.

5   At each excitation cycle the current through the
inductor 41 leads the excitation voltage and reverses its
direction before the excitation cycle ends. Thus at the
end of the excitation cycle the current flows through the
integral diode of the power switch Q_1 or Q_2 which is turned
on and which is about to close. When the upper switch Q_1
10   is closed, current still flows through its integral diode
80. When the lower switch Q_2 closes the current still
flows through upper integral diode 80; therefore it
recovers at a full DC bus voltage through a forced
recovery process, which is harsh. This forced recovery
15   process causes a momentary short circuit condition with a
high current spike (labeled in line 105 of Figure 8) and
may lead to a device failure.

The same behavior applies to the lower switch of
20   Figure 6.

The following can be observed for a capacitance
condition:

25   1.   When upper switch Q_1 is driven "Off" the
current through the inductor 41 flows into the upper
switch integral diode 80 due to current direction reversal
that occurs before the excitation ends.

30   2.   The bridge will stay at Vdd level until the
collapse of the current flowing from the inductor

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41 to the integral diode 81 or until the lower switch Q_2 is
driven into conduction.

3.   If the lower switch Q_2 is driven into
conduction while the upper switch internal diode 80 is
still carrying current, it will be driven into a harsh
recovery which may damage the device.

4.   The same phenomenon can be observed at the
lower switch Q_2 conduction period.

The problem of simultaneous conduction caused by
a harsh recovery is commonly corrected by inserting an
intentional dead time which is a period in the cycle in
which none of the switches are driven into conduction.
The dead time should be long enough to provide protection
for the switching devices, but, on the other hand,
inserting a large dead time will deteriorate the
performance of the bridge by limiting the duty cycle. It
also limits the ability of the bridge to operate near
resonance. Thus, the common solution is a compromise
offering insufficient protection at the cost of limited
performance.

In accordance with the invention, a variable
dead time is provided that adapts itself to circuit needs.
This dead time is termed a "dynamic dead time." The
dynamic dead time is achieved by sensing the point where
the current collapses to zero in a capacitive case. There
are four variants:

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                    1.   Sensing the current through the inductor 41
            by a current transformer or a shunt resistor in series
            therewith.

    5   2.   Sensing the current through the switching
            devices Q₁ and Q₂.

                    3.   Sensing the bridge voltage.

    10   4.   Sensing the rate of rise (dv/dt) of the
            bridge voltage.

                    Figure 9 shows the use of a current sense
            protection circuit in which a current transformer 110 is
    15   provided to monitor the bridge current. Figure 9 also
            shows the control module 111 which provides the LO and HO
            outputs to MOSFETs Q₂ and Q₁ respectively. This current
            measuring function can also be carried out by current
            transformers (not shown) in series with Q₁ and Q₂ or by the
    20   shunt resistor 112 in the Vss Bus. These current
            measurement devices are then connected to comparator 113
            in control module 111. Any "ringing" sensed by comparator
            113 close to the end of the current conduction period can
            be controlled by a regenerative circuit such as a Schmidt
    25   trigger, a flip-flop or a bus-holder.

                    Figure 10 shows the circuits of Figures 6 and 9
            modified for a voltage sense protection mode. Thus, in
            Figure 10, a connection is made from node 35, through
    30   resistor 115 to comparator 111.

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The operation of the circuit of Figure 10 is described in the following:

1.   An inversion of the bridge voltage at node
5   35 occurs at the point that the current collapses to zero in a case of "capacitive" operation of the bridge (line 103 in Figure 8).

2.   That inversion is sensed by means of a
10   voltage comparator (line 102, Figure 8). A dead time is inserted from the period of the switch being closed till the inversion of bridge voltage (line 102, Figure 8).

3.   Any "ringing" sensed by the comparator 113
15   near the end of the current conduction period can be controlled by a regenerative device such as a Schmidt Trigger or flip-flop or a bus holder (not shown).

4.   When the bridge operates in an inductive
20   zone (Figure 7) the inversion of the voltage occurs immediately after closing a switch; and therefore a dead time is not inserted.

Figure 11 shows a dv/dt sense protection scheme
25   which provides a capacitor 117 coupled from node 35 to a logic gate 118 within control module 111. A control module connection is provided from resistor 119 to a node between diodes 120 and 121.

30   The circuit of Figure 11 is a modification of the voltage sensing control of Figure 10 and is

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suitable for digitally controlled DC/AC Bridges. This
embodiment uses a logic gate 118 instead of the comparator
113, which is basically an analog device.

5   As long as the voltage is rising a current flows
through the sensing capacitor 117 and is clamped to VCC.
At a falling voltage capacitor 117 is clamped to the
control circuit. When the voltage of the bridge does not
rise or fall, the input of the logic gate 118 might float
10   and, therefore, it is held to an appropriate value by the
control logic.

        It is possible to use a continuous reactive load
protection arrangement in which the DC/AC bridge of Figure
15   6 is operated in a continuous capacitive regime, rather
than providing protection only.

        When the dead time is being determined
automatically by the current or voltage commutation, the
20   operation of the bridge tends to be irregular, which means
that the bridge might be driven into asymmetrical
operation and the current waveform will be irregular.

        A simple case of such an irregularity is shown
25   in the wave forms of Figure 12 which shows the curves of
Figure 8 but containing the irregularity.

        This irregular operation could be corrected by
using the previous (measured) dead time to predict a
30   minimum dead time for the cycles to come, and sense the
current or voltage afterwards, as shown in Figure 13.

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SUBSTITUTE SHEET (RULE 26)

Figure 14 shows a specific circuit diagram of a
voltage sense protection system for a fluorescent lamp
ballast (Figure 3· and 10) in conjunction with a specific
ASIC 130 for providing all control signals.

5

In Figure 14, the inversion of the bridge
voltage at node 35 is sensed by an internal voltage
comparator (within ASIC 130) at Pin CT and is used by
internal logic to expand the dead time.

10

Note that the voltage sensing method shown in
Figure 14 overcomes delays caused by bus capacitance in
the capacitive lead detection circuits.

15   Figure 15 is a block diagram of the ASIC 130,
which will later be more specifically described. Figure
16 shows the full control module, including the circuits
of Figures 14 and 15.

20   IV.   The DC to AC Inverter Bridge for Non-
                Linear Loads.

The following describes a novel process for
operating the DC to AC inverter bridge of Figure 6, which
25   drives a non-linear, resonant, and time varying load, for
example, electronic ballasts for low-pressure and high
pressure lamps, resonant power supplies, laser power
supplies, and the like.

30   There are two common control methods in use;
pulse width modulation (PWM) and frequency modulation (FM)
control. Both methods provide only partial solutions for
the problem that those power supplies

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present. The problem arises when the control circuit tries to achieve a goal of low light level (for example, very low dimming) at a small current. Trying to reach a low current using a PWM circuit could drive the DC/AC

5   bridge into the capacitive area and can lead to the destruction of the power switches Q_1 and Q_2. On the other hand trying to do so by varying the frequency usually leads to an irregular light output (rings or snakes in fluorescent lamps) and instability.

10

Although not shown in Figure 16, the various modules in ASIC 130 are interconnected within the ASIC (see Figure 15) to a central logic supervisor. The central logic supervisor controls the overall operation of

15   ASIC 130 by facilitating communications and passing data between modules.

According to the control method of the invention, both pulse width and frequency modulation are

20   employed and are constantly varied in order to dim the lamp and/or to maintain a high quality control regime. The goal is to work as close as possible to resonance but to be at the inductive behavior shown in Figure 7, under transients, lamp aging, malfunctions, use of a non-

25   compatible lamps, etc. The novel method is combined with a center tap protection solution that prevents, "pulse by pulse", being accidentally reflected into the inverter's bridge as the capacitive load, shown in Figures 12 and 13.

30   The novel algorithm for controlling the bridge when used for dimmable electronic ballasts,

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controls the preheat, ignition and dimming control
functions. In a particular case, at high light levels a
constant width pulse is used for the lower switch Q_2 of the
bridge, and a pulse of variable width is used for the
5   upper switch Q_1. This control scheme is shown in Figure 17
which shows light level as a function of pulse width Ton
for the high side and low side switches Q_1 and Q_2 in
figures 6 and 14 to 16. At the present time, low side
curve 141 is employed for constant pulse width, but any of
10   the alternates curves 142 can be used. Figure 17a further
explains the high side switch behavior shown in Figure 17.
In Figure 17a, the terms shown are defined as follows:

T	-	Full period of the half bridge
T1	-	High side switch reverse current time
T2	-	High side switch "legal direction" conduction time
T3	-	Low side switch conduction time

15

20   As explained above, the aim of the half-bridge
drive algorithm is to keep the half-bridge load inductive
but close to resonance at all operation regimes.

          The novel method is to drive the switches under
25   reverse (parallel diode) conduction, when switch voltage
is close to zero. For example, the high side drive rising
edge must come during the T1 time frame.

          The algorithm must keep time T1 short in order
30   to be close to resonance but never zero or

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negative which is the expression of capacitive load to the half bridge.

Through all operation regimes, the algorithm
provides high and low side drives that preserves a short
fixed T1. during steady state conditions. If however,
during transients the T1 shortens and gets close to zero,
then, the center tap mechanism will bring it back to a
safe length or duration.

In addition, the dead time between upper and
lower switch operation is controlled simultaneously. For
low light levels, this method is too coarse and a method
of variable width is simultaneously applied also to the
lower switch Q_2 operation.

As a general rule, the novel method allows
independent control of each one of the bridge switches Q_1
and Q_2 (or pairs of switches in case of full bridge) in a
zero voltage switching full protected mode.

The stability of the control is achieved by
changing the time constant of the DC/AC bridge control
through the different operation regimens. A small time
constant is used (fast control) when the light level is
changed on request and a larger time constant (slow
control) is used at steady state (fixed) light control.
This method avoids overshoots or undershoots and light
fluctuations respectively.

The ASIC 130 of Figures 14, 15 and 16 carries
out the control scheme described above. A further block
diagram of the silicon topology that

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controls switches Q_1 and Q_2 of the bridge, including center
tap protection is shown in Figure 18. Figure 19 shows the
control pulses produced by the circuit of Figure 18 on a
common time base.

5

       The following is a description of the operation
of the block diagram of Figure 18 and the curves of Figure
19.

10   1.   A lamp current sample is provided to
microprocessor 160 through A/D converter 161 (also
included in ASIC 130).

             2.   Microprocessor 160 processes all
15   information and provides one DATA BUS 162 that includes
all processed information (PLC, PFC, DC/AC).

             3.   Selector 163 latches appropriate data into
the appropriate LATCH 164 and 165. The rate of re-
20   latching is a decision or default of the software.

             4.   Counters "High Side PWM LOGIC" and "Low
Side PWM LOGIC" together create the HIGH SIDE waveform
(Figure 19) that can be described as a pulse train. The
25   pulse width is determined by "HS DATA" and "LS DATA" which
determine the time between pulses.

             5.   The HS waveform is fed into AND1 gate 168.
Fixed dead time and also variable dead time (determined by
30   the center tap input) is added to the waveform which then
exits through the HSDV (High Side Driver) output 169.

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6.   The waveform is also inverted by NOT3 gate 170 and fed to AND2 gate 171. Fixed and variable dead time is added to the waveform which then exits through the LSD (Low Side driver) output.

5

7.   NOT1 and NOT2 gates 173 and 174 respectively avoid the possibility of the 2 outputs HSD and LSD respectively being both "High" at the same time.

10   8.   Description of center tap protection circuit:

The outputs of AND1 and AND2 168 and 171 respectively, are monitored. If there is no overlapping with the original waveform (as getting out from HS PWM

15   Logic) for 16 consecutive pulses, then the 16 tries counter 176 increases by 1, enabling 4 consecutive cycles with no interrupting. If the same phenomenon repeats itself the 16 tries counter 176 continues to increase. If the phenomenon disappears the 16 tries counter 176 is

20   reset.

If the 16 tries counter 176 reaches 16 it sends an "Abnormal" message to the microprocessor 160 and enters an abnormal protection regime.

25

It should be noted that the above technique is applicable to a full-bridge as well as a half bridge.

In order to achieve a smooth change of light

30   output, a variable depth "dithering" technique is

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applied in the variable width pulse mechanism through the
entire lamp dimming work line.

5   Thus, using a digital control for the upper or
the lower switch pulse width by a simple PWM procedure
will cause the light to flicker. To smooth the steps of
the light control, a dithering method can be used. Thus,
a PWM of an average level which lies between PWM steps
(defined by an integer number) is composed of a mixed
10   sequence of pulses made from these two time steps.

        Precise light level control is achieved by
measuring the lamp current only. This method is
implemented by matching the current versus light-level
15   non-linear curve into linear segments. Each segment
enables a ratio between percentage of light-level and the
lamp current, allowing a very precise light level control
as shown in Figure 20. This technique avoids the need for
a complex lamp power or current measurement algorithm for
20   each type of lamp to characterize the above non-linear
behavior. Light control accuracy can be further increased
by adding additional linear segments to the matched
current versus light-level non-linear curve.

25   This method is implemented by using a dedicated
parameter table that can be set or defined by the user.
The above ratio is between the light level and the current
at certain points (the extremes of each segment).

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It is instructive to now summarize the principles adopted in algorithms used in the control method of the DC/AC inverter bridge for extreme non-linear AC load. Consider an extreme non-linear load,

5 particularly for a gas discharge lamp that behaves like a negative impedance throughout most of its dimming range. These lamps have a transfer function whose gain varies between wide limits and it is therefore difficult to attain fast and smooth control. There are two common

10 methods for controlling such a load through an AC bridge: pulse width modulation (PWM) and frequency (FM). Both are effective only within some sub-range of the load being controlled.

15 The control method described uses a PWM whose frequency and dead times are variable. It is applied in a half/full bridge topology: high side pulse width, low side pulse width with dead times between them are programmed and applied in a manner designed to achieve

20 stable, smooth control loop throughout the whole range of no load to full load.

The method used suggests working near resonance at all loads but always keeping the load just a little

25 above resonance. This is done first by providing best open loop control behavior (minimum gain variation) at every point of the load regime. Pulse width and frequency are manipulated in a manner that achieves a constant open loop gain (sometimes the PWM is used to increase load

30 current and the frequency used to decrease it and vice versa). These manipulations are performed according to the load V/I characteristics.

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The following is an example of an embodiment in a ballast application. The control of dimmable discharge lamps over the full dimming range is based on a control range that is divided into three portions by two breaking

5   points:

1.   PWM control is used from minimum load to the first breaking point: the high side pulse increases and the low side pulse decreases. The total periodic time is kept at a fixed number.

10   2.   Fix the low side and PWM the high side pulse from the first breaking point to second breaking point. The duty cycle is increased and at the same time frequency is decreased.

3.   Frequency control is used from the second

15   breaking point to maximum load both high side and low side pulses increase.

This method creates an open loop work-line with minimum gain variation and minimum predetermined dead time between pulses. This will best control a predictable load

20   (e.g., a lamp with normal operating behavior). In order to prevent failures caused by unpredictable behavior of the load, the center-tap voltage of the bridge is sampled to ensure that switching is at zero voltage. Pulses are dynamically changed to protect against destructive

25   currents. Dead time is increased dynamically to the zero voltage point. This feature of the method enables working at high frequencies with very short predetermined dead time for a lamp with normal operating behavior. In addition, its permits increasing the dead time in the

30   event of transients and changes in load behavior, for example, as the discharge lamps age.

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V.   A Digital Implementation of a Power
      Control Circuit.

The following describes various techniques
employed in the novel digital approach to power
5   management controllers, in particular to a dimmable
electronic ballast. Figure 21 shows the power line
carrier (PLC) controlled dimmable ballast of layout
similar to that shown in Figure 16. The ballast
control ASIC 200 is shown within the solid line block
10   200 in Figure 20. PLC operation allows the ballast to
receive dimming control information across the same
power line being used to power the ballast. ASIC 200
is in turn schematically shown in Figure 21A. The
ASIC Pin assignments are shown in Figure 22. The wall
15   control unit (W.C.U.) schematics are also shown in
Figure 23. The techniques used in Figures 20, 21 and
22 are generally described as follows:

I.   Feed Forward Dynamic Response
      Adaptation Based on Energy Consumption
20   Prediction

The dynamic response of the control loop is
"flexible". It will use a different "dumping factor"
& loop response time for a number of pre-decided
conditions. For example the following decisions table
25   is applied in the case of the electronic ballast:

If DC bus voltage is within the limits of
Vref+-1% then "no response";
If DC bus is within the limits of +-
3%>Vref>+-1% then "slow" response;

If DC bus is within the limits of +-10%>Vref>+-
3% then "fast" response;
If step light level + if under 90% of desired
then fast response;

5   If input voltage step changed more than +-2%
then fast response, etc.

If a large change of the light is desired, the
desired light level is first given to the controller, as
10   for example, going from full light to light off (transient
mode), then the PFC operation mode will be switched to
fast response in order to avoid DC bus dips. At constant
light (steady state) the PFC control switches to slow
response mode preventing light flickering/glimmering.
15

Limits, dumping factors and response times are
parameters listed in predefined designer programmable
tables.

20   The control can be adjusted to handle all kinds
of applications, including motor control, temperature
control and many others.

II. <u>Programmable Parameter Tables</u>
25

Tables of parameters are programmed for all
possible regimes of the needed application. For example,
in the electronic ballast case there are about 12
different regimes for the Dimmable Electronic Ballast,
30   including:

DC bus soft start;

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                    Auxiliary build up;

                    Lamp preheat;

                    Lamp ignition;

                    Up going light level;

5   Down going light level;

                    Step up light level;

                    Step down light level;

                    Steady state "high" load;

                    Steady state "low" load;

10   Abnormals - output power shut-down; and

                    Input voltage switched off - or "black

outs."

         Every single regime has its own specific

15 parameters table that is chosen when entering a new

regime.

         Each parameter table contains all the special

parameters for PFC control and DC/AC bridge control for

20 each specific regime. The designer can program these

parameters.

         In order to maintain a stable DC bus and the

best PFC at all regimes, a digital control using

25 programmable look-up tables gives the best "treatment" to

each different regime (i.e. in the DC/AC bridge inverter

control case the response time changes according to the

lamp regimen operation).

30   With this approach, the more complicated the

application, the more efficient the digital solution.

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III. Adaptive Loop Parameters

Static and dynamic loop response adapt
themselves to the inputs by getting feedback information
5   from a number of digital and/or analog inputs chosen
according to the right parameter tables, decision tables
and addressed equations.

IV.   Idle Periods Insertion to Change to
10   Discontinuous Mode for Low Power Loads,
             Keeping Frequency Within Desired Limits
As loads get smaller, frequency gets very high
and "ON" pulses have to be very short in order to preserve
critical mode conduction. Under a certain load, critical
15   mode becomes impractical. At this point the control
changes to "Discontinuous" mode and it stops controlling
the "ON" time and begins controlling the "OFF" time of the
pulse. The "ON time" is fixed to a desired "minimum
usable pulse" (programmable parameter). "Off time" can
20   change between none and "Discontinuous mode maximum dead
time" (programmable parameter).

V.   A Method for Controlling the Converter at
      No Load Conditions by Means of Implementing
25   a Special "Stand By" PWM Regimen Mode Using
      Dedicated Programmable Parameters Table

Special modes of operation can be "tailored" by
using digital programmed control. All parameters,
30   including: "pulse width", time between pulses, burst
parameters and other parameters can be assigned for a
specific task.

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One example of this ability is the "stand by" mode which we use for the electronic ballast.

This mode is operational any time the ballast
5   output stage is inhibited and the PFC stage must carry on its operation in standby mode. At this mode the PFC stage has two tasks: first - to provide the auxiliary voltages 5V and 12V to the control and second - to keep the DC bus voltage within limits.

10

When the PFC stage has very small load, the DC bus capacitor will charge rapidly to a nominal limit and will inhibit PFC control pulses. Special parameters are used in order to allow the PFC stage to provide auxiliary
15   voltages: minimum pulse width and fixed dead time between pulses. Another mode of operation is to change from controlling the DC bus (except for maximum) to controlling the auxiliary voltage to 12V.

20   VI.   Protection Method by Combining Multiple
                   Parameter Levels Using Programmable Tables.
                   _____

The parameter tables also contain some limits to
25   provide part of the protections. For example: control pulses will be inhibited (pulse-by-pulse) in case of DC bus over-voltage (the pulses are inhibited if the DC bus is higher than 110%). Also, if input voltage is above a certain predetermined limit, pulses will be inhibited.
30   Input under-voltage is also monitored; the PFC control will go to power

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shutdown mode under a predetermined limit (over-voltage protection (OVP) in the present ASIC implementation).

The PFC theory and parameters, are described as
5   follows:

MinPFCParam
Max. PFC Ton pulse for Max load at Min Input RMS voltage
Ton=(255-n)/12MHz
10   100   1.29E-05   Sec
MaxPFCParam
Minimum usable Pulse for PFC control
125   4.17E-07   Sec
LowDelPrs
15   Discontinuous mode Maximum Dead time.
      0   2.13E-05 Sec
HighDelPrs
At Critical mode only.
When getting ZC signal, waits 83 more nsec to activate PFC
20   switch.
254   8.33E-08   Sec
ShutHighDelPrs
Fixed Dead time in Shut Down mode.
150   8.75E-06   Sec
25   ### DampingFactor
1 / Control Speed. control step={[(Vref-VDC)/n]+1}*83nsec
14
MaxVDC
Software ShutDown PFC Ton pulse will go off when VDC
30   crosses this reference.

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245   439.5 Volt

>VDCRef

2.19 Volt (A/D level)   This is the normal VDC reference.

223   400 Volt

5   VdcHys1

Range of steady state.   At VDCRef+/-n PFC Ton pulse will

not change.

2   3.6 Volt

>VdcHys1

10   Demand for fast response, fast PWM at VDC+-VdcHys1 or

higher.   When error is between VdcHys and VdcHys1, there

will be a slow response.   PWM=Fast

14   25.1 Volt

>PfcPWMPrs

15   Slow PWM response factor.

20

>PfcPWM1Prs

Fast PWM response factor (0 when no PWM).

0

20   MinPFCStartUp

Soft Start. Width of PFC Ton pulse when dc bus voltage

climbs from zero to VDC.

253   1.67E-07 Sec

>PFCTimerPRs

25   "Slow" Loop response = 100mSec. Every 10msec, counter

increased by 1.

10

>PFCLoopCounterPRs

"Fast" Loop response = 1mSec. Every 250usec, counter

30   increased by 1.

4

Sampling rate of VDC

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Fixed at 500usec.

Linkage between PFC and DC/AC: for step new
light, PFC is "FAST" up to 90% of new light, and then
becomes "SLOW" between 90% and 100% of new light.   "90%"
5 is not included as a parameter.

When changing the light by "UP" or "DOWN" PFC
control is always "SLOW".

DcAc Paramaters:
10   ***********************

DcAcHvs
Range for Fast/Slow response when Curr. Ref. is higher
then 75.   When Curr. Ref. is lower then 75, there is only
slow response.   Under 2 there is no change in Ton pulse.
15 2 is not included as a parameter.
5   1.96%

SlowDcAcPrs
Slow response PWM of 20 possible combinations of last and
next Ton (HSD).   Pulse may change every 250usec.
20 20

FastDcAcPrs
Fast response PWM of 5 combinations.   Pulse may change
every 250usec.
5

25   StartDcAcPrs
Response for DcAc StartUp (PWM) climbing to start up light
after ignition.
15

HSD
30 Ton pulse changes always through all workline points.
StartTon
HSD Ton Pulse for lamp ignition.
175 6.67E-06   Sec

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<u>StartTonTime</u>

Duration of HSD Ton Pulses for lamp.

ignition=2*250usec=500usec

2   500   uSec

5   Very fast Climbing to StartTon with NOPWM.

<u>AbDelayPrs</u>

Wait after shut down Shut Down period.

200   2   Sec

<u>ShutTimerPrs</u>

10   Wait after shut down Shut Down period.

200   2   Sec

<u>EBCurrentRef</u>

Lower Current reference for lower power dissipation on

shunt resistor (EB).

15   51   1   Volt

<u>LightLevel(6)</u>

Table for IR Light decoding =n/2

"0,2,30,80,150,200"   "0,1,15,40,75,100"%

<u>LightBasePrs(4)</u>

20   Fix points on lamp curve - 15,40,65,100% Lamp current must

be provided for each percentage point."

"30,80,130,200"   "15,40,75,100"%

<u>CurrentBase4</u>

Volt 100% Light REFERENCE for ALL LIGHT LEVELS

25   227   2.23

<u>MaximumLightLevel</u>

Ballast Factor.

200   100 %

<u>Accessories Parameters:</u>

30   ******************************

<u>MaxLightSensor</u>

If n=251 to 255 then occupancy switch closed.

250   2.45   Volt

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MinStartDC

For DC control. If value is under 10(5%) then power
shutdown

10   5   %

5   PLC Parameters:

                    ****

            NoiseHys1

Digital filter for PLC after summation stage.

10

10   GlobalZone

                    0

            TrxFreq(4)

PLC frequencies. F=3ee06/(64-n)

"33,34,35,36" ."96.77,100,103.44, 107.13" kHz

15

            The following is a lead assignment and function
description for the ASICS of Figures 15 and 21 and the
control module of Figure 16:

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
RESET, LINE SYNC, PROTECTION & P.I.C. PINS					
1	RST	**Reset Schmidt Trigger Input**			
		Reset Input of the Control Module, Control Module is in Reset state until Input reaches VIH level (2.2X-3.5V). Reset action is automatic. Reset Initialization Process is completed about 200 msec after Power on.	pull-up	200	KOhm
			Capacitance	0.47	uF
			Threshold	2.2-3.5	Volt
2	LINE	**Line Phase Schmidt Trigger Input**			
		Line Phase Input (see Ballast Platform Diagram for connection manner of LINE pin).	Positive Threshold	2.2-3.5	Volt
			Negative Threshold	1-2.2	Volt
			Frequency	47-63	Hz.
3	SD	**Shut-down Schmidt Trigger Input**			

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Pin No	Name	Function	Parameter	Value	Units
		Shut-down (Protection) Input for Abnormal Operation Protection. When voltage goes high, LSD&HSD immediately disables for 2 seconds. The controller tries to start the operation again at normal start-up routine. If Abnormal situation still exists it will shut-down again. After 10 attempts with 2 sec. intervals between attempts, Half Bridge Drive signals (HSD & LSD Outputs) are permanently inhibited (low level). If No Failure Operation lasts above 2 seconds, the Counter of 10 attempts resets (zero value).	Positive Threshold	2.2-3.5	Volt
			Negative Threshold		Volt
			Min Pulse Width		uSec
			Max Delay Time		uSec
4	PLC	Power Line Carrier Comparator Input			
		Power Line Carrier (PLC) Remote Control data input. The following operations can be done via PLC Communication: Dimming, Ballast Turn on, Ballast Turn off & Zone Select.	Frequency Range	95-105	KHz
			Threshold	1.67	Volt
			pull-up	100	KOhm

PFC SECTION

| 5 | ZC | Zero Current Schmidt Trigger Input | | | |

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
		Zero Current (ZC) pulse (High to low edge) Switch-On Time period.	Positive Threshold	2.2-3.5	Volt
			Negative Threshold	1-2.2	Volt
6	PFCD	PFC Drive Digital Output			
		PFC Drive signal Drives the PFC switch driver.	Min High	4.5	Volt
			Max Low	0.3	Volt
			Max Sink	5	mAmp
			Max Source	5	mAmp
7	CL	Current Limiter Comparator Input			
		Current Limiter Comparator limits (pulse-by-pulse) PFC Switch current by comparing PFC Switch Current Sample to 2.5V. When pin voltage exceeds 2.5V PFCD turns to low until the next PFC Cycle.	Threshold	2.5	Volt
			Pull-up	100	KOhm
8	REF	Current Reference Comparator Input			
		User Adjustable Current Reference Voltage compared to CL pin Voltage. Used to calibrate the PFC to minimum Input Line Current THD.	Max Ref.	0.4	Volt
			Min Ref.	0.2	Volt
			Pull-up	100	KOhm

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Pin No	Name	Function	Electrical Data (VCC=5V) Parameter	Value	Units
POWER SUPPLY & REFERENCE SECTION					
9	GND	GND Power Supply Input			
		The GND of the 5VDC supply is also reference for all Control Module signals	Max Current	50	mAmp
10	VCc	VCC Power Supply Input 5VDC supply to the control module	VCCmax	5.1	Volt
			VCCmin	4.9	Volt
			Ivcc max	44	mAmp
A/D ANALOG INPUT SECTION					
General		All Analog Inputs are connected to 8 bit A/D Converter via 4 inputs Analog Selector. The A/D Reference Voltage is 2.5V. Input Voltage between 2.5V to VCC converts to 255 Digital Value. The Digital Converted Value is: $\#D = 255 * V_{ANALOG}/2.5$ (Integer 8 bits)			
11	CNFG	Ballast Configuration Analog Input	DC Range	0-0.24	Volt
		Analog input is used to define 5 Ballast Configurations by different Voltage Level Limits. See Configuration Table 1 for details. CNFG Voltage is sampled during Reset Initialization Process to determine Ballast Configuration. CNFG Pin is ignored during Ballast operation after the initialization.			
			Occupancy	0.25-0.73	Volt
			PLC Range	0.74-1.22	Volt

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SUBSTITUTE SHEET (RULE 26)

Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
			Local Range	1.23-1.71	Volt
			E.B. Range	1.72,2.5-1.71	Volt
			Pull-up	100	KOhm
12	ZONE	Zone Select/Analog Input			
		Analog input used:			
		1) to define 8 Ballast Zone at PLC Configuration, by different voltage Level Limits. See Zone identification Table 2 and PLC D.E.B section for detail	Zone Range Width	0.25	Volt
			All Zone	0-0.25	Volt
			Zone 1 Range	0.25-0.5	Volt
			Zone 7 Range	1.75-5	Volt
		2) to determine Light Level at DC configuration, by voltage Level See DC D.E.B. section for details	Max Light	2.22	Volt
			Zero Light	Parameter	digital
		3) as Light Sensor Analog Feedback Input at Local Configuration. See LOCAL D>E>B> section for details	Max Level	2.2	Volt
			Min Level	0.2	Volt

Pin			Electrical Data (VCC=5V)		
No	Name	Function	Parameter	Value	Units
13	VDC	4) to determine Low Light Level at Occupancy Configuration, by voltage Level. The % Light Level is determined according to formula: %Light=(V_{ZONE} 2.23)x100 At Occupancy, ZONE pin is sampled at transit from normal light to (non) occupancy. See Occupancy D.E.B. section for details			
		PFC stage, output DC bus voltage Analog Feedback Input			
		Analog Feedback input for PFC output DC bus voltage. This voltage is Software Compared to 2.23VDC (the Converted Value Compared to #227) predefined reference, to provide the DC/AC stage with the required DC voltage. (The Feedback Loop stabilizes the VDC Pin to 2.23VDC.)	0% Light	Customer determines the expected ILAMP Voltage for each of these 4 fixed points (By PDK Software)	
			15% Light		
			40% Light		
			65% Light		
			100% Light	2.23	Volt
DC/AC SECTION					
15	HSD	High Side Switch Driver Signal Digital Output			

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
		5V Pulse Modulated Drive Signal to High Side switch of the DC/AC Driver	Max Current	5	mAmp
			Min High	4.5	Volt
			Max Low	0.3	Volt
16	LSD	Low Side Switch Driver signal Digital Output	Max Current	5	mAmp
		5V Pulse Modulated Drive Signal to Low Side switch of the DC/AC Driver	Min High	4.5	Volt
			Max Low	0.3	Volt
17	CT	Center Tap Voltage sample Schmidt Trigger Input			
		The Center Tap voltage sample from Half Bridge center tap is used to keep Half Bridge at Zero Voltage Switching mode and to match the HSD & LSD timing to keep the Half Bridge Load's inductive character.	Positive Threshold	2.2-3.5	Volt
			Negative Threshold	1-2.2	Volt

DIGITAL INPUTS

		All Digital Inputs, except IR, are sampled during Reset Initialization Process and ignored during Ballast operation after the Initialization			
		The following data is related to all Digital Inputs. Pull-up is semiconductor type	Min High	2.4	Volt
			Max Low	0.8	Volt

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
18	IR	Infrared Control Digital Input			
		Infrared Control Digital input signal used to control Light Level y Digital Code in LOCAL configuration only.	Pull-up	7.5 to 8	KOhm
SO-S3: Parameters Tables Select Digital Inputs					
19	SO	Desired Parameters Table is selected by 4 bit hexadecimal. Code 0-12 selects one of 13 Internal Predefined Parameter Tables. Code 13 selects EEPROM Parameter Table. Code 15 selects Programming Mode of EEPROM Parameters Table. Code 14 is not applicable	Pull-up	30 to 40	KOhm
20	S1				
21	S2				
22	S3				
23	STP	Step-by-Step operation Digital Input.			
		Input enables Step by Step operation of the Ballast. Digital "low" activates Step by Step operation mode. Momentary Digital "high" forwards to the next step.	Pull-up	30 to 40	KOhm
		Step 0 (Reset): Before any Digital "high" pulse to STP Pin. No Drive pulses from PFCD, HSD & LSD pins.			

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
		Step 1: Operates PFC stage operation only			
		Step 2: Operates Lamp Preheat			
		Step 3: Lamp Ignition & Steady State Operation			
24	DLCTR	Inhibits Center Tap Protection. Digital Active Low Input			
		Digital "Low" to DLCTR Pin Inhibits Center Tap Protection Facility for Ballast development only. (Refer to PDK Manual)	Pull-up	30 to 40	KOhm
25	NOT APPLICABLE				
26	LOD	Local Oscillator Driver Digital Output			
		Local Oscillator Driver 46.9KHz fixed frequency digital square wave is available immediately after Reset.	Max Current	5	mAmp
			Min High	4.5	Volt
			Max Low	0.3	Volt
			Duty Cycle	0.5	
			Frequency	46.9	KHz
27	TX	Parameters Programming Transmitter Digital Output			

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Pin No	Name	Function	Electrical Data (VCC=5V)		
			Parameter	Value	Units
		TX Pin is used as a transmitting output for RS232 Communication using Parameters Development Kit (PDK, SI/PDK-02) during Programming Mode.	Min High	4.5	Volt
			Max Low	0.3	Volt
			Max Sink	1	mAmp
			Max Source	1	mAmp
28	RCV	Parameters Programming Receiver Digital Input RCV Pin is used as Receiving input for RS232 Communication using Parameters Development Kit (PDK, SI/PDK-02) during Programming Mode. RCV Pin is also used as Occupancy signal input at Occupancy and Local configurations. (see Local D.E.B. and Occupancy D.E.B. sections for details)	Min High	2.4	Volt
			Max Low	0.8	Volt
			Pull-up	30 to 40	KOhm

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The following is a description of operating voltages and the like for the ASIC 200 and Control Module:

MAXIMUM RATINGS

Units	Max	Min	Parameter Definition	Symbol
V	5.5	-0.5	DC Supply Voltage (Referenced to GND)	VCC
mAmp	50		DC Supply Current, VCC & GND pins	ICC
V	vCC+0.5	-0.5	Pick Inputs Voltage, Referenced to GND (RST, LINE, SD, PLC, ZC, CL, CREF. CNFG, ZONE, VDC ILAMP, CT, IR. S0, S1, S2, S3, STP, DLCTR, RCV.)	Vout
V	VCC+1	-1	Pick outputs Voltage Referenced to GND (PFCD, HSD, LSD, DCLK, PLCD, XMT.)	Iout
mAmp	+5	-5	Pick outputs Current (PFCD, HSD, LSD. PLCD)	Iout1
mAmp	+1	-1	Pick outputs Current (DCLK. XMT)	Iout2
mW	275		Power Dissipation	PD
°C	+150	-55	Storage Temperature	Tstg
°C	260		Lead Temperature	TL

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)	4.9	5.1	V
ICC	DC Supply current, VCC & GND pins	36	44	mAmp
Vin (A)	Analog Inputs Voltage (CNFG, ZONE, VDC, VLAMP)	0	2.5	V
Vin (D)	Digital Inputs Voltage (All other inputs)	0	VCC	V
Vout	Output Voltages (PFCD, HSD, LSD, DCLK, PLCD, XMT.)	0	VCC	V
TAMB	Ambient Temperature	0	70	°C

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ELECTRICAL CHARACTERISTICS

VCC=5V unless Test Conditions are different

Sec.	Type	Pin Name	No.	Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Power Supply										
	Power Supply	VCC	10	UVLO	Under-voltage Lock Out voltage	4.3	4.5	4.7	V	Vcc Applied, Vcc Disabled
				ICC	Supply current	39	43	47	mA	
Reset										
	Digital Input	RST	1	VRST	Pin voltage at steady state	4.5	4.9	5	V	
				TRST1	Hard Reset Time (4)	65	100	150	nSec	
				TRST2	Total Reset Time (5)	165	200	250	nSec	
Interrupt										
	Schmidt Trigger Input	LINE	2	VIH	Positive going Input Threshold	2.5		3.5	V	
				VIL	Negative going Input Threshold	1		2.2	V	
				FLINE	Operational Frequency	47	50/60	63	Hz	
Protection										

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			Parameter	Description				Units	Conditions
Schmidt Trigger Input	SD	3	VIH	Positive going Input Threshold	2.5	2.7	3.5	V	
			VIL	Negative going Input Threshold	1		2.2	V	
			SDPW	Minimum Pulse Width to activate SD protection				uSec	
PLC Communication									
Comparator Input with 100k Pull-Up	PLC	4	VPLC	Voltage at PLC input	4		5	V	Open input
			PLC REF	Comparator Internal Reference Voltage		1.67		V	Vcc=5.0V
PFC									
Schmidt Trigger Input	ZC	5	VIH	Positive going Input Threshold	2.5		3.5	V	
			VIL	Negative going Input Threshold	1		2.2	V	
Digital Output	PFCD	6	VOH	High level voltage of PFC pulse	4.5	4.9	5	V	10pF load
			VOL	Low level voltage of PFC pulse	-0.3	0	0.3	V	10pF load
			IO	Output Current Sink & Source		5		mA	

Type	Symbol	Pin	Parameter	Param. Symbol	Min	Typ	Max	Units	Notes
			Maximum applicable PFC Ton Pulse-Width	TonMax		12.9[1]	66[2]	uSec	
			Minimum applicable PFC Ton Pulse-Width	TonMin		0.42		uSec	
			Maximum applicable PCF Dead time (Discontinuous mode)	TofMax		21.3[1]	66[2]	uSec	
Comparator Input with 100k Pull-Up	CL	7	Current Limit Comparator Internal Reference Voltage	CLREF		2.5		V	
Comparator Input with 100k Pull-Up	CREF	8	Voltage at comparator input (Fine Tuning of Minimum THD)	VCREF	0.2		0.4	V	Adjusted by user

A/D Analog Inputs Section

Type	Symbol	Pin	Parameter	Param. Symbol	Min	Typ	Max	Units	Notes
Analog Input	CNFG	11	Open Analog Input Voltage (Analog Input with Internal 100k Pull-Up)	Vopen	4.5	4.9	5	V	open input
Analog Input	ZONE	12	Operation Analog Input	Voper	0		2.5	V	set by voltage divider
Analog Input	VDC	13							
Analog Input	ILAMP	14							

DC to AC Section

Type	Symbol	Pin	Parameter	Param. Symbol	Min	Typ	Max	Units	Notes
Digital Output	HSD	15	High level value of HSD output	VHSD	4.5		5	V	10pF load

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Category	Symbol	#	Parameter	Min	Typ	Max	Unit	Notes
	TonMax		High limit of HSD Ton Pulse Width	0.37		20.4	uSec	(3)
	TonMin		High limit of HSD Ton Pulse Width	0.37		20.4	uSec	(3)
	TonWU		Ton Pulse Width	0.37		20.4	uSec	(3)
	TonIGN		Ton Pulse Width	0.37		20.4	uSec	(3)
Digital Output	LSD	16	High level value of LSD output	4.5		5	V	10pF load
	LSDTon		Ton Pulse Width	0.37		20.4	uSec	(3)
Schmidt Trigger Input	CT	17	Positive going Input Threshold	2.5		3.5	V	
	VIL		Negative going Input Threshold	1		2.2	V	
Digital Inputs								
Digital Input With Internal 7.5K Pull-Up	IR	18	Voltage at IR Open Input	4.8	4.98	5	V	open input
Digital Input	SO	19	Voltage at Digital Open Input	4.5	4.98	5	V	open input
With Internal	S1	20						
30K to 40K	S2	21						
Pull-Up	S3	22						
	STP	23						

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	DLCTR	24							
Local Oscillator/Output Driver									
Digital Output	LOD	26	FLOD	Frequency of LOD output		46.9	5	KHz	
			VLOD	Amplitude of LOD output	4.5	5	5	V	10pF load
Serial Communication Section									
Digital Output 7.5K Pull-Up	XMT	27	VXMT	Amplitude Voltage of XMT output	4.5	4.98	5	V	10pF load
Digital Input 5K Pull-Up	RCV	28	VRCV	Voltage at RCV open input	4.5	4.98	5	V	open input

Notes:

(1) Numbers are subject to Customization

(2) Reaching its maximum value at Line Zero Cross, under Max Load and minimum input Line RMS voltage

(3) EEPROM Programmable Parameters. El_Char.doc

(4) C20 (See CONT_B.Sch) Charge Time to Schmidt Trigger Input Positive going Input Threshold (VIH).

(5) C20 Charge Time + Software Delay Time

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The following is an operation description which describes control module 111 and ASIC 200 settings:

Customer Selectable Parameters for D.E.B. Applications

The customer can influence ballast behavior by
5   determining several ballast parameters. Software is used
to determine the ballast parameters. The customer
parameters below describe these parameters.

Customer Parameters Table

No.	Parameter Name	Parameter Description	Possible Range	Rational Range	Units
Frequency Parameters					
1	Low Switch Ton	Required LSD Pulse Width			
2	Minimum High Switch Ton	Required Minimum HSD Pulse Width			
3	Maximum High Switch Ton	Required Maximum HSD Pulse Width			
Lamp Curve Parameters					
4	Minimum Light	Expected Minimum Lamp Current Sense Voltage VILAMP(mim			
5	15% Light	Expected 15% Lamp Current Sense Voltage VILAMP (15%)			
6	40% Light	Expected 15% Lamp Current Sense Voltage VILAMP (40%)			
7	65% Light	Expected 15% Lamp Current Sense Voltage VILAMP (65%)			
Warm-up Parameters					
8	Warm-up High Switch Ton	Required Warm-up HSD Pulse Width			

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9	Time	Required Warm-up Time			
Light Parameters					
10	Minimum Light	Required Minimum % Light Level			
11	Start Up Light	Re			
Ignition Parameters					
12	Ignition High Switch Ton	Required Ignition HSD Pulse Width	0.37-20.37	2-13	
13	Ignition Time	Required Ignition Time	0-25	0-25	mSec
14	Post Ignition High Switch Ton	Required Post Ignition HSD Pulse Width	0.37-20.37	1-13	

5

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Parameters Tables Selection

     The control module 111 contains 13 parameters
tables in its PROM and one customer parameters table in
its EEPROM. Only the manufacture can change the
5 parameters of tables 0-12. The customer can program its
own parameters in EEPROM Table 13 using a Parameter
Development Kit (PDK).

     Tables 0-3: Versions for two T8-32W (parallel
configuration) lamps (120V line application). Tables 4-
10 12: Versions for two T8-36W (parallel configuration)
lamps (230V line application).

     Of course, customization of internal parameter
tables is possible. A desired parameter table is selected
by combination of micro-jumpers S0, S1, S2, S3 (connected
15 to S0-S3 pins) to create a hexadecimal number. Insert
jumper for a logic "0", and leave open for logic "1". The
Parameter Tables Selection Table below defines the
selection of the desired parameters table.

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Parameters Tables Selection Table

Table	S0	S1	S2	S3	Function
0	0	0	0	0	Select parameters from one of 13 Pre-Defined Tables in the PROM
1	1	0	0	0	
2	0	1	0	0	
3	1	1	0	0	
4	0	0	1	0	
5	1	0	1	0	
6	0	1	1	0	
7	1	1	1	0	
8	0	0	0	1	
9	1	0	0	1	
10	0	1	0	1	
11	1	1	0	1	
12	0	0	1	1	
13	1	0	1	1	Select parameters from EEPROM Parameters Table
14	0	1	1	1	Reserved for Internal Use
15	1	1	1	1	PDK Programming mode. Disable Ballast Operation and enable EEPROM Parameters Table Programming by PDK.

5

10

15

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Selected Ballast Configuration Options: Selected via A/D
Input CNFG

        Control module 111 and ASIC 200 enable ballast
operation in 5 different configurations as follows:

5   PLC D.E.B.   Ballast is remote controlled from Wall
                      Control Unit with Power Line Carrier (PLC)
                      interface. In PLC configuration, the
                      ballast can be designated as belonging to
                      one of 7 different zones or as belonging to
10   all zones. Ballast zone designation is
                      selected via A/D input ZONE. (See PLC
                      D.E.B. Section below).

    DC D.E.B.   Ballast is controlled from DC Wall Control
                      Unit via DC lines. (See LOCAL D.E.B.
15   Section below).

    LOCAL D.E.B.   Ballast is controlled from local infrared
                      IR light & occupancy sensors. (See LOCAL
                      D.E.B. Section below).

    Occupancy
20 D.E.B.   Ballast is controlled from local occupancy
                      sensor. (See occupancy D.E.B. Section
                      below).

    E.B.   Non Dimmable Electronic Ballast. (See E.B.
                      Section).

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The Ballast Configuration Table shows, ballast configuration selection via the CNFG pin. To get the required configuration, connect a resistor between CNFG pin and GND.

5

Ballast Configuration Table

Configuration	PLC	DC	Occupancy	Local	E.B.
CNFG Voltage Range	0.73-1.22	0-0.24	0.25-0.73	1.23-1.71	1.71-2.5
Converted Digital Value	75-125	0-25	25-75	125-175	175-255
Recommended Resistor (5%)	30KΩ	0Ω	13KΩ	51KΩ	130KΩ

10

PLC D.E.B.

Start up

15   The ballast starts lamps at "last light level" (saved on the EEPROM). The light level stays in Last Light Level until a dimming command is sent from the wall Control Unit via PLC communication.

PLC Function

20   The ballast receives a 17-bit string from the Wall Control Unit (W.C.U.) via PLC Remote Controlled Communication. Bit allocation is as follows:

       1 bit   -   Start

       2 bits   -   Control operation modes

25   3 bits   -   7 Selected zones

       6 bits   -   64 light level

       4 bits   -   Check Sum

       1 bit   -   Spare

The rate of communication is 1 bit per line cycle. PLC
communication is synchronized to the line phase.

Ballast Zone Identification

5   Designation of the ballast zone identity (0-7)
is implemented by providing a voltage in equal equidistant
increments between 0 to 2.5V to the zone pin. The Zone
Selection Table is shown below.

Zone Selection Table

Zone	All Zone	1	2	3	4	5	6	7
Center Voltage	0.125	0.375	0.625	0.875	1.125	1.375	1.625	1.875
Voltage Range	0-0.25	0.25-0.5	0.5-0.75	0.75-1	1-1.25	1.25-1.5	1.5-1.75	1.75-2

EEPROM Function

15   When "Line Disappeared" is detected, (via the
line pin) the present light is saved as "last light level"
in the EEPROM. When the ballast is switched on it will
revert to this "last light level". When "Table 15" (S0,
S1, S2, S3 = "1") is selected, the EEPROM can be
20 programmed to a desired parameters table. When Table 13
is selected, the parameters table is obtained from the
EEPROM.

DC D.E.B.

Start Up

25   The ballast starts the lamps according to the
last light level from the EEPROM parameters table and then
increases or decreases to the DC controlled light level
present in the ZONE pin. This DC level is applied from
the DC control unit. The light level is

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related to ZONE pin voltage according to the following
formula:

Light Level=(ZONE pin Voltage/2.23V)xMaximum Light Level

5   The maximum light level is obtained when the
ZONE pin Voltage is 2.23V (converted to 227).

The lamp light goes to 0 when the ZONE pin
voltage drops under 110mV. The Ballast starts-up when
ZONE pin voltage exceeds 140mV.

10   LOCAL D.E.B.
Start Up
The ballast will start the lamps according to
the last light level saved in the EEPROM parameters table.

Local IR Function
15   The IR receiver output signal is connected to
the IR pin.
The IR transmitter sends 8 codes: 5 Preset light
levels, Up, Down and Off commands.

Light Sensor Function
20   The ballast light level is controlled by a light
sensor connected via the ZONE pin. The ZONE pin is
feedback input converted to a digital number and compared
to the sensor reference value.

The Sensor Reference value is set to the light
25   sensor (ZONE pin) value during reset

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initialization. In the case of constant voltage at the
ZONE pin (open loop), the light level stays at the last
light level (no error detected - Sensor Reference = ZONE
pin voltage, and no dimming UP or DOWN command is
5 generated).

        The dimming command from the IR transmitter
changes the sensor reference and changes the light level
by a controlled close loop mechanism to get:

    Light Sensor = New Sensor Reference.
10 Light Sensor voltage range is 0.2V to 2.45V.

Occupancy Function (at Local Configuration)
        Two inputs serve the occupancy function:

        The "Occupancy OFF" command uses the RCV pin.
Logic "1" (open circuit) at the RCV pin detected as a "No
15 Presence" and turns the ballast off. Logic "0" at the RCV
pin is detected as "presence" and starts-up the ballast to
last light value.

        The ZONE analog input pin is also used as a "No
Presence Inhibit". If ZONE pin Voltage > 2.5V then "No
20 Presence" disabled. The ballast dims the light to the
minimum light level.

        After the occupancy sensor detects a presence in
the room, the ballast returns to the last light level.
There is no delay time between "No Presence" detection (by
25 the control module) and the dimming operation.

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<u>Occupancy D.E.B.</u>

Start up

     Ballast will start lamps according to last light
level saved in the EEPROM parameters table.

5   <u>Occupancy Function</u>

     The RCV pin serves as a "Presence Detection"
input. When "No Presence" detected (logic "High"-open
circuit) at the RCV pin, the ballast dims the light to the
defined "Dim Light Level" on the ZONE pin. The dim light
10 level is saved at the "No Presence Detected" moment
according to following formula:

Dim Light Level=[Maximum Light Level]x[ZONE Voltage at
Initialization Time] 2.23V.

     The ballast returns to the maximum light level
15 after occupancy sensor detects a presence in the room
(logic "0" at ZONE pin).

Note: There is no delay time between "No Presence"
detection (by Control Module) and the dimming operation.

<u>EB</u>

20 **Start up**

     Ballast will start lamps to "Maximum Light
Level".

E.B. Function

     The ballast operates only at the maximum light
25 level. Dimming is not possible. As in all other
configurations, the lamp current is stabilized

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by closed loop control via the ILAMP feedback input pin. The ILAMP pin voltage is 0.5V at the maximum light level situation.

Housekeeping/Protection Circuits

5   Four input pins of the control module 111 and ASIC 200 are used for the protection functions of the ballast.

The CL input is used for current limit protection of PFC switch. The PFCD output pin (PFC Drive
10 Pulse Signal) is pulse-by-pulse inhibited when the CL input exceeds 2.5V.

The VDC A/D input pin is used for closing the DC bus (PFC Output) loop and also as a hardware over- voltage
15 protection sense input. (Input to analog comparator). The PFCD output is pulse-by-pulse inhibited when the VDC pin voltage exceeds 2.5V. Also, the VDC input is used for software over-voltage protection. Alternatively, the PFCD output is pulse-by-pulse inhibited (by software) when the
20 VDC pin voltage exceeds 2.4V.

The CT input is used to keep the half bridge at a zero voltage switching (ZVS) operation. If the load becomes capacitive, the CT input will partially block the
25 HSD or LSD outputs (increase dead times in order to keep ZVS operation). If the limitation causes total disappearance of HSD pulses 16 times, then 4 cycles are enabled without interfering with the CT input. This total cycle of 20 (16+4) will repeat

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itself 16 times and if the malfunction does not disappear,
it will activate the abnormal function.

    The SD input is used to sense catastrophic
failures of the ballast. When the SD input exceeds the
5   Schmidt Trigger positive going threshold (2.2V-3.5V)
according to catastrophic ballast failure occurrence, then
hardware immediately inhibits (shuts down) theHSD & LSD
outputs and software activates the abnormal function. The
controller will try to start-up the ballast again 2
10 seconds after shutdown. If no abnormal indication is
detected 2 seconds after ignition of the lamps, the
abnormal protection procedure automatically resets an
internal failure counter. If the failure is still
detected, the controller will try to start-up the ballast
15 10 times with 3 second intervals between attempts. After
10 tries, the HSD & LSD outputs will be permanently
inhibited. CT protection is also monitored as a
catastrophic failure.

    An abnormal condition of CT protection initiates
20 the same abnormal protection procedure.